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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/631,804	08/01/2003	Naoki Kubo	Q76384	1990

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SUGHRUE MION, PLLC
2100 PENNSYLVANIA AVENUE, N.W.
SUITE 800
WASHINGTON, DC 20037

EXAMINER	
WILLIAMS, ALEXANDER O	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 05/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/631,804	KUBO	
	Examiner	Art Unit	
	Alexander O Williams	2826	

-- The MAILING DATE of this communication appears on the cov r sheet with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4, 6-13 and 15 to 24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-13 and 15-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/9/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/631804 Attorney's Docket #: Q76384
Filing Date: 8/1/2003; claimed foreign priority to 8/2/2002

Applicant: Kubo

Examiner: Alexander Williams

Applicant's Amendment filed 3/23/04 has been acknowledged.

Claims 5 and 14 have been canceled.

Receipt is acknowledged of papers submitted under 35 U.S.C. § 119, which papers have been placed of record in the file.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 to 4, 6 to 13, 15 to 21 and 24 are rejected under 35 U.S.C. § 102(b) as being anticipated by Walz (U.S. Patent # 5,307,237).

1. Walz (figures 3 and 4) specifically figure 4 show an IC package comprising: an IC chip **300**; a substrate **302** including a conductive layer **306**; a heat-radiating mechanism **308** that is mounted on the substrate, disposed between the IC chip and the substrate, and dissipates heat of the IC chip; and an insulating layer **(portion between306 and 308 of 302)** between the heat-radiating mechanism and the conductive layer of the substrate, wherein the heat-radiating mechanism and the conductive layer of the substrate are electrically connected via connection members **304** disposed in plural through-holes disposed in the insulating layer, and wherein terminals of the IC chip and the heat-radiating mechanism are electrically connected **(by 324)**.

2 and 18. The IC package of claim 1 or 9, Walz show wherein the IC chip is fixed on the heat-radiating mechanism **(through 310)**.

3. The IC package of claim 1, Walz show wherein the IC chip and the heat-radiating mechanism are electrically connected by wire bonding **324**.

4. The IC package of claim 1, Walz show wherein the IC chip and the heat-radiating mechanism are electrically connected by a conductive material **324**.

6. The IC package of claim 1, Walz show wherein the terminals of the IC chip are ground terminals and the conductive layer **306** is a ground layer.

7. The IC package of claim 1, Walz show wherein the terminals of the IC chip are power terminals and the conductive layer **306** is a power layer.

8. The IC package of claim 1, Walz show wherein the heat-radiating mechanism **308** comprises a heat sink.

Claims 9 and similar claim 24. Walz (figures 3 and 4) specifically figure 4 show an IC package comprising: an IC chip **300**; a substrate **302** including a conductive layer **306**; a heat-radiating mechanism **308** that is mounted on the substrate, disposed between the IC chip and the substrate, and dissipates heat of the IC chip, wherein the heat-radiating mechanism comprises plural heat sinks **308,316,322**, and at least part of each heat sink is disposed below the IC chip, and wherein terminals of the IC chip and the heat-radiating mechanism are electrically connected **(by 324),** and the heat-radiating mechanism and the conductive layer of the substrate are electrically connected **(by 304)**.

10. The IC package of claim 9, Walz show wherein the plural heat sinks **308,316,322** are disposed so as to be separate from each other.

11. Walz (figures 3 and 4) specifically figure 4 show a connection structure comprising: an IC chip **300**; a substrate **302** disposed with a conductive layer **306**; a heat-radiating mechanism **308** that is mounted on the substrate, disposed between the IC chip and the substrate, and dissipates heat of the IC chip, an insulating layer **(portion between 306 and 308 of 302)** between the heat-radiating mechanism and the conductive layer of the substrate, wherein the heat-radiating mechanism and the conductive layer of the substrate are electrically connected via connection members **304** disposed in plural through-holes disposed in the insulating layer, and wherein terminals of the IC chip are electrically connected to the conductive layer via the heat-radiating mechanism.

12 and 19. The connection structure of claim 11 or 9, Walz show wherein the IC chip and the heat-radiating mechanism are electrically connected by wire bonding **324**.

13 and 20. The connection structure of claim 11 or 9, Walz show wherein the IC chip and the heat radiating mechanism are electrically connected by a conductive material **324**.

15. Walz (figures 3 and 4) specifically figure 4 show a method of connecting an IC chip **300** and a substrate **302** including a conductive layer **306** sandwiched between insulating layers **(within 302)**, the method comprising the steps of:

(a) disposing a heat-radiating mechanism **308** between the IC chip and the substrate;

(b) fixing the IC chip to the heat-radiating mechanism (thorough 310);

(c) disposing plural through-holes **304** in at least one of the insulating layers (within **302)**; and

(d) disposing connection members **304** in the through-holes so that the heat-radiating mechanism and the conductive layer of the substrate are electrically connected via the connection members.

16. Walz (figures 3 and 4) specifically figure 4 show an electrical device disposed with an IC package that includes: an IC chip **300**; a substrate **302** including a conductive layer **306**; a heat-radiating mechanism **308** that is mounted on the substrate, disposed between the IC chip and the substrate, and dissipates heat of the IC chip, an insulating layer **(portion between 306 and 308 of 302)** between the heat-radiating mechanism and the conductive layer of the substrate, wherein the heat-radiating mechanism and the conductive layer of the substrate are electrically connected via connection members **304** disposed in plural through-holes disposed in the insulating layer, and wherein terminals of the IC chip are electrically connected **(by 324)**.

17. Walz (figures 3 and 4) specifically figure 4 show an electrical device disposed with a connection structure that includes: an IC chip **300**; a substrate **302** disposed with a conductive layer **306**; a heat-radiating mechanism **308** that is mounted on the substrate, disposed between the IC chip and the substrate, and dissipates heat of the IC chip, an insulating layer **(portion between 306 and 308 of 302)** between the heat-radiating mechanism and the conductive layer of the substrate, wherein the heat-radiating mechanism and the conductive layer of the substrate are electrically connected via connection members **304** disposed in plural through-holes disposed in the insulating layer, and wherein terminals of the IC chip are electrically connected to the conductive layer via the heat-radiating mechanism.
21. Walz further show an insulating layer **(portion between 306 and 308 of 302)** between the heat-radiating mechanism and the conductive layer of the substrate, wherein the heat-radiating mechanism and the conductive layer of the substrate are electrically connected via connection members **304** disposed in plural through-holes disposed in the insulating layer.

Claims 1 to 4, 6 to 13, and 15 to 24 are rejected under 35 U.S.C. § 102(e) as being anticipated by Roh et al. (U.S. Patent # 6,521,990 B2).
1. Roh et al. (figures 1 to 3) specifically figure 2 show an IC package **100** comprising: an IC chip **10**; a substrate **20** including a conductive layer **31**; a heat-radiating mechanism **30** that is mounted on the substrate, disposed between the IC chip and the substrate, and dissipates heat of the IC chip; and an insulating layer **21** between the heat-radiating mechanism and the conductive layer of the substrate, wherein the heat-radiating mechanism and the conductive layer of the substrate are electrically connected via connection members 40-43 disposed in plural through-holes disposed in the insulating layer, and wherein terminals **12a,12** of the IC chip and the heat-radiating mechanism are electrically connected **(by 50)**.
2 and 18. The IC package of claim 1 or 9, Roh et al. show wherein the IC chip is fixed on the heat-radiating mechanism.
3. The IC package of claim 1, Roh et al. show wherein the IC chip and the heat-radiating mechanism are electrically connected by wire bonding **50**.
4. The IC package of claim 1, Roh et al. show wherein the IC chip and the heat-radiating mechanism are electrically connected by a conductive material **50**.

6. The IC package of claim 1, Roh et al. show wherein the terminals **12a** of the IC chip are ground terminals and the conductive layer **31** is a ground layer.
7. The IC package of claim 1, Roh et al. show wherein the terminals **12** of the IC chip are power terminals and the conductive layer **32** is a power layer.
8. The IC package of claim 1, Roh et al. show wherein the heat-radiating mechanism **30** comprises a heat sink.
Claims 9 and similar claim 24. Roh et al. (figures 1 to 3) specifically figure 2 show an IC package **100** comprising: an IC chip **10**; a substrate **20** including a conductive layer **31,32**; a heat-radiating mechanism **30,34** that is mounted on the substrate, disposed between the IC chip and the substrate, and dissipates heat of the IC chip, wherein the heat-radiating mechanism comprises plural heat sinks **30**, and at least part of each heat sink is disposed below the IC chip, and wherein terminals of the IC chip and the heat-radiating mechanism are electrically connected **(by 50),** and the heat-radiating mechanism and the conductive layer of the substrate are electrically connected **(by 40a-43)**.
10. The IC package of claim 9, Roh et al. show wherein the plural heat sinks **30** are disposed so as to be separate from each other.
11. Roh et al. (figures 1 to 3) specifically figure 2 show a connection structure 100 comprising: an IC chip **10**; a substrate **20** disposed with a conductive layer **31,32**; a heat-radiating mechanism **30** that is mounted on the substrate, disposed between the IC chip and the substrate, and dissipates heat of the IC chip, an insulating layer **21** between the heat-radiating mechanism and the conductive layer of the substrate, wherein the heat-radiating mechanism and the conductive layer of the substrate are electrically connected via connection members **40a-43,25** disposed in plural through-holes disposed in the insulating layer, and wherein terminals of the IC chip are electrically connected to the conductive layer via the heat-radiating mechanism.
12 and 19. The connection structure of claim 11 or 9, Roh et al. show wherein the IC chip and the heat-radiating mechanism are electrically connected by wire bonding **50**.
13 and 20. The connection structure of claim 11 or 9, Roh et al. show wherein the IC chip and the heat radiating mechanism are electrically connected by a conductive material **50**.
15. Roh et al. (figures 1 to 3) specifically figure 2 show a method of connecting an IC chip **10** and a substrate **20** including a conductive layer **31,31** sandwiched between insulating layers **21**, the method comprising the steps of:

(a) disposing a heat-radiating mechanism **30** between the IC chip and the substrate;
(b) fixing the IC chip to the heat-radiating mechanism;
(c) disposing plural through-holes **40a-43,** in at least one of the insulating layers **21**; and
(d) disposing connection members **25** in the through-holes so that the heat-radiating mechanism and the conductive layer of the substrate are electrically connected via the connection members.

16. Roh et al. (figures 1 to 3) specifically figure 2 show an electrical device disposed with an IC package 100 that includes: an IC chip **10**; a substrate **20** including a conductive layer **31,32**; a heat-radiating mechanism **30** that is mounted on the substrate, disposed between the IC chip and the substrate, and dissipates heat of the IC chip, an insulating layer **21** between the heat-radiating mechanism and the conductive layer of the substrate, wherein the heat-radiating mechanism and the conductive layer of the substrate are electrically connected via connection members **40a-43,25** disposed in plural through-holes disposed in the insulating layer, and wherein terminals of the IC chip are electrically connected **(by 50)**.

17. Roh et al. (figures 1 to 3) specifically figure 2 show an electrical device disposed with a connection structure that includes: an IC chip **10**; a substrate **20** disposed with a conductive layer **31,32**; a heat-radiating mechanism **30** that is mounted on the substrate, disposed between the IC chip and the substrate, and dissipates heat of the IC chip, an insulating layer **21** between the heat-radiating mechanism and the conductive layer of the substrate, wherein the heat-radiating mechanism and the conductive layer of the substrate are electrically connected via connection members **40a-43,25** disposed in plural through-holes disposed in the insulating layer, and wherein terminals of the IC chip are electrically connected to the conductive layer via the heat-radiating mechanism.

21. Roh et al. further show an insulating layer **21** between the heat-radiating mechanism and the conductive layer of the substrate, wherein the heat-radiating mechanism and the conductive layer of the substrate are electrically connected via connection members **40a-43,25** disposed in plural through-holes disposed in the insulating layer.

22. Roh et al. shoe the conductor layer is a ground layer **31** and another conductor payer **32** is a power layer.

23. Roh et al. further include an insulating layer **21** between the heat radiating mechanism **30** and the conductor layers **31,32** of the substrate, wherein said first of said plural heat sinks **30** and the ground layer **31** are electrically connected via a first set of

connection members **40a** disposed in plural through holes disposed in insulating layer, and wherein said second of said plural members **25** disposed in plural through holes disposed in insulating layer.

Response

Applicant's arguments filed 3/23/04 have been fully considered, but are moot in view of the new grounds of rejections detailed above.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/684,796,666,698,696,675,784,786,692,693,691,712, 713,717,720	12/12/03 5/24/04
Other Documentation: foreign patents and literature in 257/684,796,666,698,696,675,784,786,692,693,691,712, 713,717,720	12/12/03 5/24/04
Electronic data base(s): U.S. Patents EAST	12/12/03 5/24/04

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AOW
5/25/04

Primary Patent Examiner
Alexander O. Williams